COURSE PROFILE

Course Number : EE 242	**Course Title :** Logic Circuit Design Laboratory
Required / Elective : Required	**Pre-requisite :** - **Corequisite:** EE 240
Catalog Description: Experiments with logic gates and combinational circuits, digital arithmetic circuits, multiplexers, flip-flops, counters, shift registers.	**Textbook / Required Material :** Logic Design Lab. Manual
Course Structure / Schedule : (0+0+2) 1 / 2 ECTS	
Extended Description : This is a required laboratory course for the Computer and Electronics Engineering students. The goal of the course is to give students a hands-on experience in design, implementation, and debugging of digital circuits and prepare students for the design of practical digital hardware systems using Verilog.	
Design content :-	**Computer usage:** VHDL (Verilog Hardware Description Language)

Course Outcomes:

A student who successfully completes the course will be able to

- Construct and analyze small multi-level combinational logic circuits containing AND, OR, NOT, NAND, NOR, and XOR gates.[5],[6],[7]
- Analyze and design modular combinatorial logic circuits containing decoders, multiplexers, demultiplexers, 7-segments display decoders and adders. [5],[6],[7]
- Analyze and design of sequential circuits using the concepts of state and state transition. [5],[6],[7]
- Represent and simulate a logic circuit using Verilog. [5],[6], [11]
- Develop basic laboratory skills, recording of data, and write well-organized technical reports. [5],[6],[9]
- Present their application projects via oral and visual media. [9],[11]
- Have an ability of professional and ethical responsibility.[4]
- Learn to work in team, responsibilities of circuit construction.[8]

Level of contribution of course to program outcomes:
Strong: [5],[6],[8]
Average: [4],[7],[9],[11]
Some: -

Recommended reading:

Digital Design, Third Edition, M. Morris Mano, Prentice-Hall, ISBN : 0-13-062121-8

Contemporary Logic Design, Randy H. Katz, Benjamin/Cummings Publishing, ISBN:0-8053-2703-7

Teaching Methods:

Pre-readings, preliminary works, lecture and group work.

Assessment Methods:

Laboratory reports, class survey in lab., term project, preliminary works

Student Workload:

Preparatory reading and pre-works	7 hrs
Homeworks, laboratory reports	10 hrs
Projects	2 hrs
Laboratory work	28 hrs
Final Exam	3 hrs
TOTAL …… 50 hrs … to match 25 x 2 ECTS	

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